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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,315	12/02/2003	Scott Van De Graaff	M4065.1001/P1001	2707

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,315	GRAAFF ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,12-19,22-27,30-33,36-40,43-48,51-53,56,57,60-68,71 and 74-76* is/are rejected.

7)☒ Claim(s) *2,3,10,11,20,21,28,29,34,35,41,42,49,50,54,55,58,59,69,70,72 and 73* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

1. Claims 1-76 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 02 December 2003. The information disclosed therein was considered.

Specification

3. Claims 16-18 and 38 are objected to because of the following informalities:

Claims 16-18 recite "said circuit", and it is not clear which circuit it is referring to (since there are the low power control circuit, the buffer circuit and the differential circuit). It will be understood as --said low power control circuit--.

Claim 38 depends on claim 37 which appears to be in error. In view of Fig. 2, claim 38 will be understood to depend on claim 27.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4-9, 12, 14, 15, 19, 22-27, 30-33, 36, 38-40, 43-48, 51-53, 56, 57, 60-68, 71 and 74 are rejected under 35 U.S.C. 102(e) as being anticipated by Schoenfeld et al. (U.S. Pat. No. 6,816,994).

Regarding claims 1, 4, 5, 15, 27, 39 and 48, Schoenfeld, for example in Figs. 3 and 6, discloses a low power control circuit in a memory device and a processor, and a related method, for transitioning a memory device between a first operating mode (power up mode) and a low power operating mode (power down mode), said low power control circuit comprising: a differential circuit (differential amplifier 608) connected to a reference voltage (VREF) and a first control signal (XCKE); and a buffer circuit (inverter 604) having an input connected to the first control signal (XCKE); wherein in the first operating mode said differential circuit is used to detect a first value of the first control signal (XCKE going low) and causes a transition from the first operating mode to the low power operating mode (by generating a low CKEINT), and in the low power operating mode said buffer circuit and said differential circuit are used to detect a second value of the first control signal (XCKE going high) and cause a transition from the low power operating mode to the first operating mode (see for example column 5, line 21 through column 7, line 18).

Regarding claims 6, 7, 19, 22, 26, 30, 31, 40, 43, 47, 51, 57, 60, 64 and 65, Schoenfeld further discloses a first logic circuit (including 648 and 644 and the logic elements used to generate ENTTL and PWRDWN) connected to the differential circuit (via ENDIFF) and the buffer circuit (via ENTTL), said first logic circuit disabling the buffer circuit and enabling the differential circuit in the first operating mode (see for example column 7, lines 4-8), and in the

low power mode, enabling the buffer circuit and disabling the differential circuit until the buffer circuit detects the second value (see for example column 5, lines 64-67);

and a second logic circuit (including 632, 652 and 628) coupled to the outputs of the buffer circuit and the differential circuit, said second logic circuit combining the outputs of the buffer circuit and the differential circuit to form an output (CKEINT) causing the memory device to transition between the first and low power operating modes (see for example column 6, lines 46-48).

Regarding claims 8, 9, 23-25, 32, 33, 44-46, 52, 53, 61-63, 66-68, Schoenfeld, in Fig. 6, discloses that no current is applied to said differential circuit when disabled, or said differential amplifier is completely choked when disabled (i.e., interpreted broadly to represent either turning ON or OFF of current to 608 to either enable or disable 608);

a reduced current is applied to said differential circuit when disabled, or said differential amplifier is partially or mostly choked when disabled (i.e., interpreted broadly to include inherent leakage current in 608).

Regarding claims 12, 14, 36, 38 and 56, Schoenfeld, in Fig. 6, further discloses that said first logic circuit is connected to receive at least a second control signal indicative of a low power operation, wherein said low power operation is a power down operation (signal PWRDWN).

Regarding claims 71 and 74, Schoenfeld, in Fig. 6, further discloses a step of ensuring that the first control signal has the second value, wherein said ensuring step comprises comparing the first control signal to the reference voltage once it is determined that the first

control signal has the first value (by enabling 608 via ENDIFF so that 608 compares XCKE to VREF).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 13 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schoenfeld et al. (U.S. Pat. No. 6,816,994) in view of Qureshi et al. (U.S. Pat. No. 5,793,776).

Schoenfeld discloses a circuit and a method as in claims 12 and 27, with the exception of said low power operation being a self refresh operation. Qureshi discloses a self refresh operation for a low power operation (see for example column 1, lines 63-67).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the circuit and the method of Schoenfeld with the activation of a self refresh operation, since it was well known in the art (as disclosed in Qureshi) that a self refresh operation is commonly activated as a low power operation.

8. Claims 16-18, 75 and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schoenfeld et al. (U.S. Pat. No. 6,816,994) in view of Kajigaya et al. (U.S. Pat. No. 5,539,692).

Schoenfeld discloses a circuit and a method as in claims 1 and 71, with the exception of said low power control circuit being configured to perform low power control via programming

an antifuse or setting a switch in a metal mask, or configured to ignore the reference voltage via an antifuse. Kajigaya discloses use of antifuses and fuses (impliedly including metal masks) for mode setting (see for example column 16, lines 16-23).

Since use of antifuses or metal masks (or fuses) as a configuration means was common and well known in the art (as disclosed in Kajigaya), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to configure the low power control circuit of Schoenfeld via programming an antifuse or setting a switch in a metal mask, for the purpose of providing a flexibility means for setting additional or optional features in a device, especially after fabrication or packaging of the device.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 4, 5, 15, 27, 37-39, 48 and 56 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 39, 40 and 42-44 of U.S. Patent No. 6,816,994 ("Patent") in view of Jang (U.S. Pat. No. 6,058,063) and Qureshi et al. (U.S. Pat. No. 5,793,776).

Claims 39, 40 and 42-44 of Patent recites a low power control circuit for transitioning a memory device between a first operating mode and a low power operating mode, said low power control circuit comprising: a differential circuit (a first higher power buffer, in claims 39 and 40 of Patent) connected to a first control signal (a clock enable signal, in claim 44 of Patent); and a buffer circuit (a lower power buffer, in claim 39 of Patent) having an input connected to the first control signal (a clock enable signal, in claim 43 of Patent); wherein in the first operating mode (power up) said differential circuit is used to detect a first value of the first control signal and causes a transition from the first operating mode to the low power operating mode (implied in claim 44), and in the low power operating mode (power down) said buffer circuit and said differential circuit are used to detect a second value of the first control signal and cause a transition from the low power operating mode to the first operating mode (implied in claims 43 and 44); wherein said buffer circuit comprises an inverter (claim 42 of Patent); wherein said low power operation is a power down operation (claim 39 of Patent).

The Patent does not recite a reference voltage connected to the differential circuit, that the differential circuit is a differential amplifier, and the low power operation is a self refresh operation.

However, Jang, for example in Figs. 2 and 3, discloses a differential amplifier (201) with a reference voltage (Vref) to detect a control signal (CSB), and Qureshi discloses a self refresh operation for a low power operation (see for example column 1, lines 63-67).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to connect a reference voltage to the differential circuit claimed in Patent to detect the clock enable signal in Patent, since use of differential amplifiers with a reference

voltage connected to detect a control signal was common and well known in the art. Further, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the circuit claimed in Patent with the activation of a self refresh operation, since it was well known in the art that a self refresh is commonly activated as a low power operation.

Allowable Subject Matter

10. Claims 2, 3, 10, 11, 20, 21, 28, 29, 34, 35, 41, 42, 49, 50, 54, 55, 58, 59, 69, 70, 72 and 73 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 2, 3, 20, 21, 28, 29, 41, 42, 49, 50, 58, 59, 69, 70, 72 and 73, the prior arts of record do not disclose or suggest a low power control circuit as recited in claim 2, 3, 20, 21, 28, 29, 41, 42, 49, 50, 58, 59, 69, 70, 72 or 73, and particularly, the reference voltage being grounded or floated during the low power operating mode.

Regarding claims 10, 11, 34, 35, 54 and 55, the prior arts of record do not disclose or suggest a low power control circuit as recited in claim 10, 11, 34, 35, 54 or 55, and particularly, a current reduced by about twenty-five or seventy-five percent of full current is applied to said differential circuit when disabled (i.e., intentionally reduced to about 25% or 75% of full current).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

ANH PHUNG
PRIMARY EXAMINER